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Seat Number .....

Name .....Student ID.....

Midterm Examination Semester 1 Year 2017

Course: CPE 223 Digital Electronics and Logic Design **Group 31, 32**

Date: 29, September, 2017 13.00-16.00

Instruction

1. Calculator, books, documents, and notes are not allowed in the examination room.

2. Carefully read the explanation in each problem and then answer each question.

3. Do not take the examination sheets out of the examination room.

4. This examination has 13 pages including this page (6 problems, 40 points).

- Student must raise your hand to ask for permission before leaving the room.
- Student must not take the exam and booklet outside the room.
- The highest punishment can be applied if the cheating is discovered.

(Asst. Prof. Suthathip Maneewongvatana, Ph.D.)

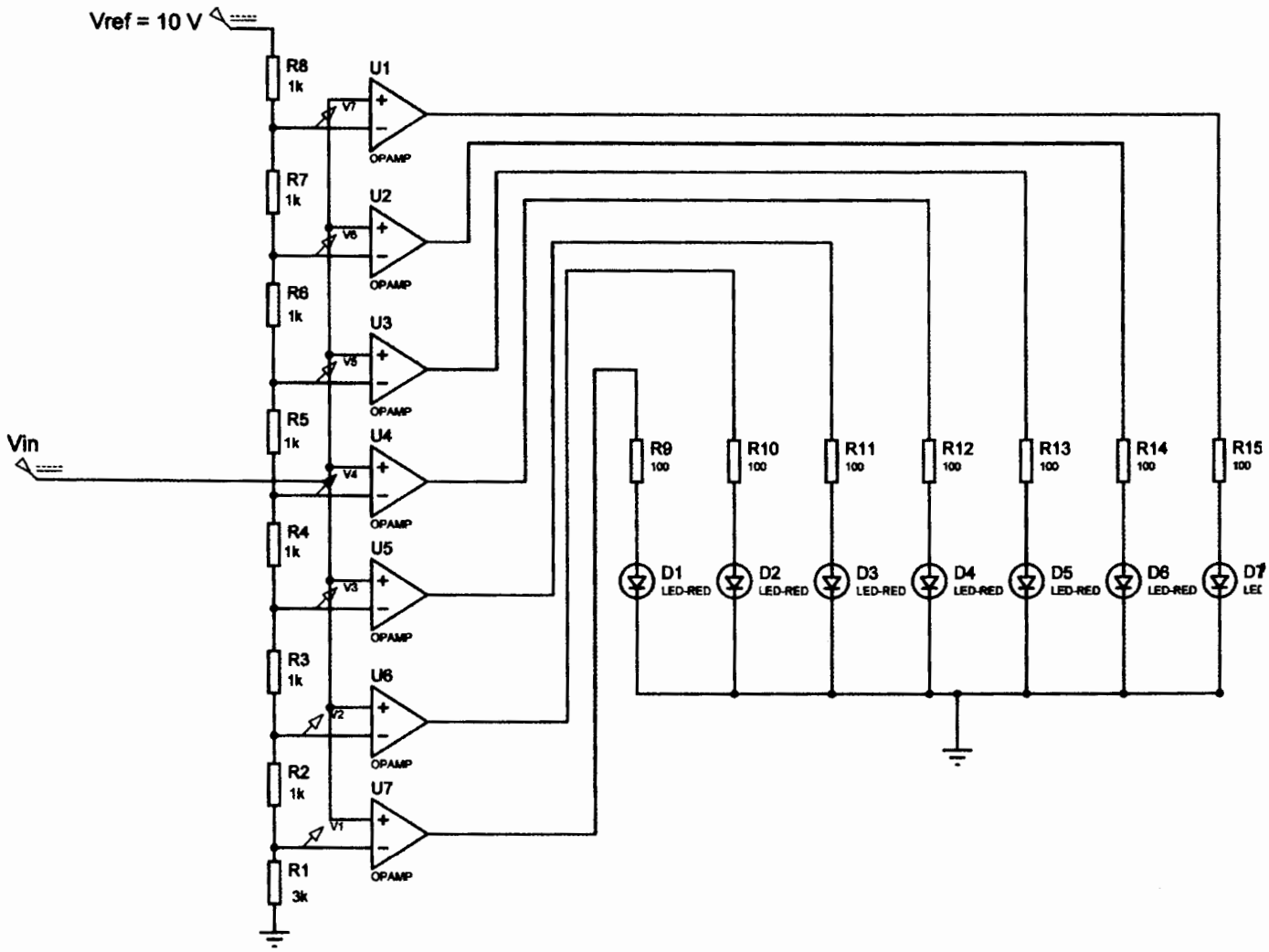
This exam is approved by the Computer Engineering Department's committees

(Assoc. Prof. Dr. Natasha Dejdumrong)

Program chair

Date.....Month.....Year.....

1. Consider the circuit below: **(8 points)**



a) Identify the voltage level measured at position v1-v7 (4 points)

Position	Voltage Level (Volt)
v1	
v2	
v3	
v4	
v5	
v6	
v7	

b) Which LED(s) will be bright if the voltage level for Vin = 5.2 V, and 6.25 V, respectively (2 points)

c) What is the range of Vin to turn on all LEDs? (2 points)

2. For the following Boolean functions: **(6 points)**

a. $F(W,X,Y,Z) = \sum m(1,5,6,7,11,12,13,15) + D(9,14)$ Simplify the Boolean function F into Sum of Products form. (2 points)

b. $F(A,B,C,D) = \sum m(0,1,3,4,5,7,8,9,12)$ Simplify the Boolean function F and implement the circuit by using only NOR gates (4 points)

3. Show the steps of addition or subtraction (use 2's complement representation) between two 4 bit binary numbers A and B. Indicate whether an overflow occurs. **(3 points)**

   a) A+B given A= 0011, B=0111 (1 point)

   b) A-B given A=0011, B=1001 (1 point)

   c) A+B given A=0101, B=1110 (1 point)

4. Figure 1. represents 7-segment (*A-G*) displaying number 0-9 (0000-1001) and A-F (1010-1111).

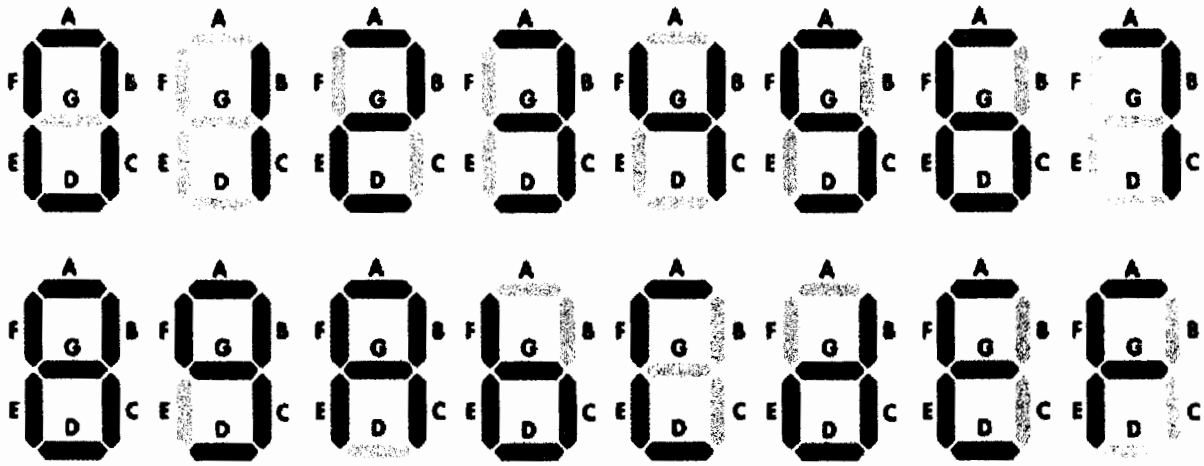


Figure 1

(12 points)

a) Write the truth table representing 4bit binary input and the outputs for only two segments (segment A and B) using a common Anode 7-segment. (4 points)

b) Minimize the Boolean function in SOP form to generate the output for segment *A* and *B*. (2 points)

c) Implement the circuit to drive segment *A* of a common Anode 7-segment using two 3 to 8 Decoders (74LS138 see in datasheet) and NAND gates (6 points)

5. Consider Boolean function $f(w_1, w_2, w_3) = (w_1 + w_2)(w_2 + \overline{w_3})(\overline{w_1} + w_3)$. **(6 points)**

a) Write the truth table for this function (1 points)

b) Implement the circuit of this function by using:

i) NAND gates only (1 points)

ii) A 2-to-1 multiplexer using w_1 as a selector and other necessary gates. (2 points)

iii) A 3-to-8 decoder and other necessary gates. (2 points)

6. The circuit in Figure 2 looks like a counter. **(5 points)**

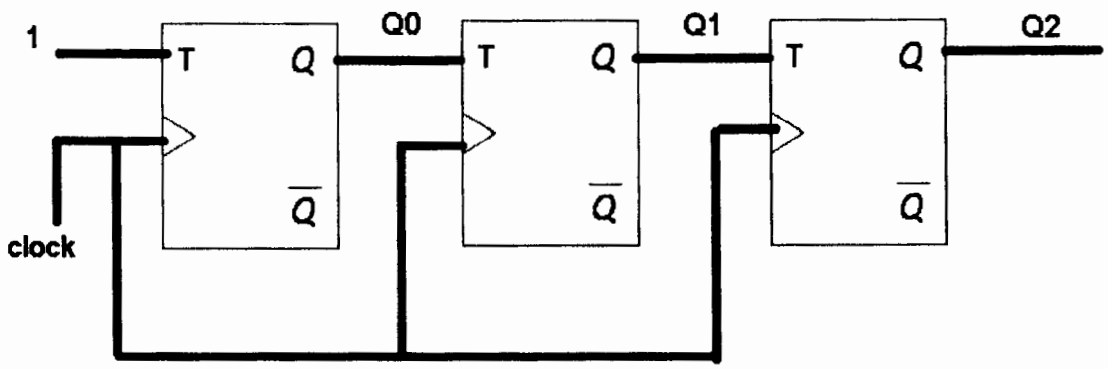
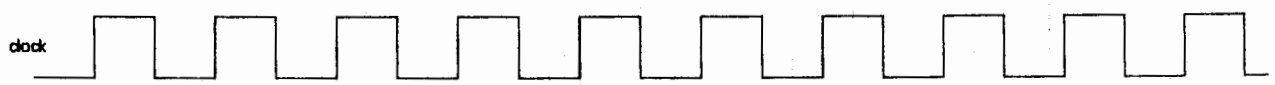


Figure 2

a) Draw the timing diagram representing clock, Q0, Q1, and Q2 (4 points)



b) What is the sequence that this circuit counts? (1 points)

MOTOROLA

1-OF-8 DECODER/ DEMULTIPLEXER

SN54/74LS138

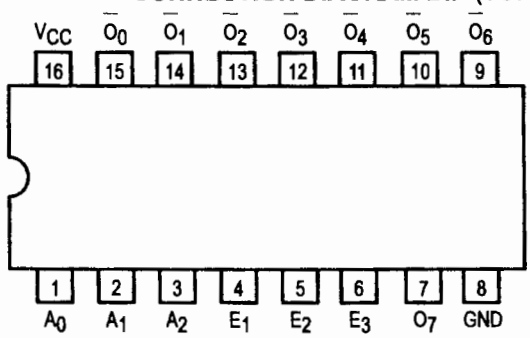
1-OF-8 DECODER/ DEMULTIPLEXER

LOW POWER SCHOTTKY

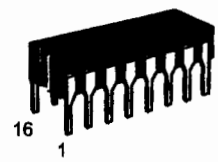
The LSTTL/MSI SN54/74LS138 is a high speed 1-of-8 Decoder/ Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Typical Power Dissipation of 32 mW
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

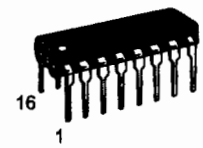
CONNECTION DIAGRAM DIP (TOP VIEW)



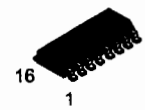
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

PIN NAMES

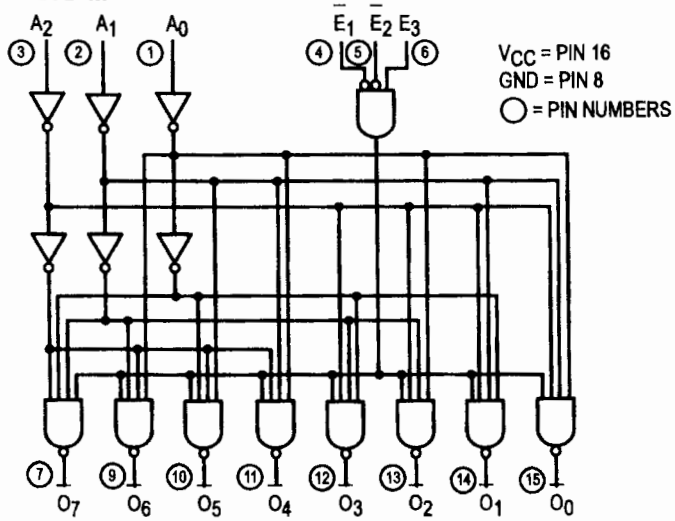
		LOADING (Note a) HIGH	LOW
$\overline{A_0}$–$\overline{A_2}$	Address Inputs	0.5 U.L.	0.25 U.L.
E_1, E_2	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
O_0–O_7	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

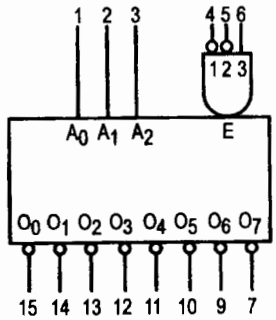
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC DIAGRAM



LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

FUNCTIONAL DESCRIPTION

The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW Outputs ($\overline{O}_0 - \overline{O}_7$). The LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

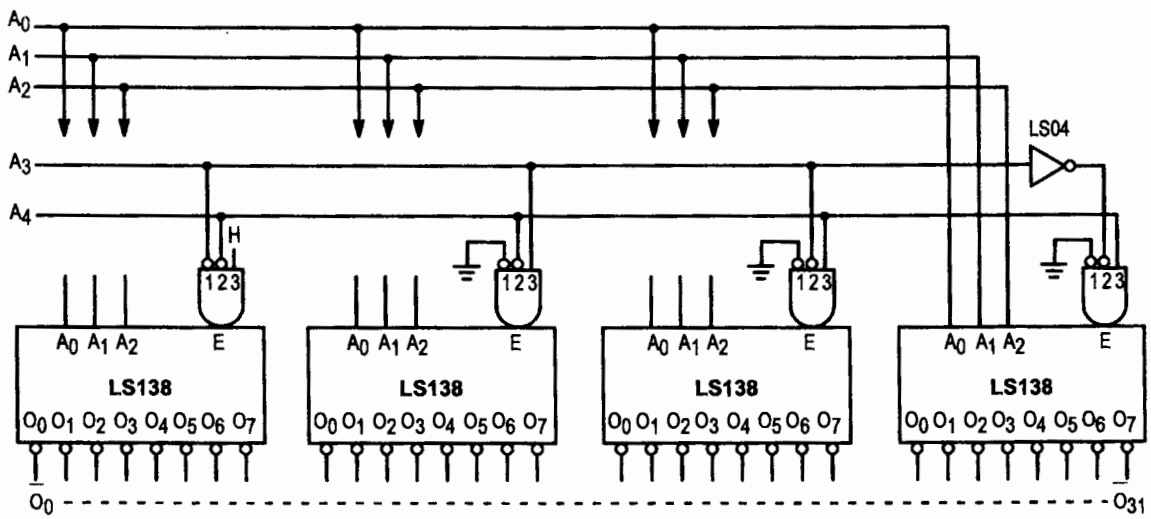


Figure a